MAR 0 1 2004
PATENT & TRADEMARK OFFICE

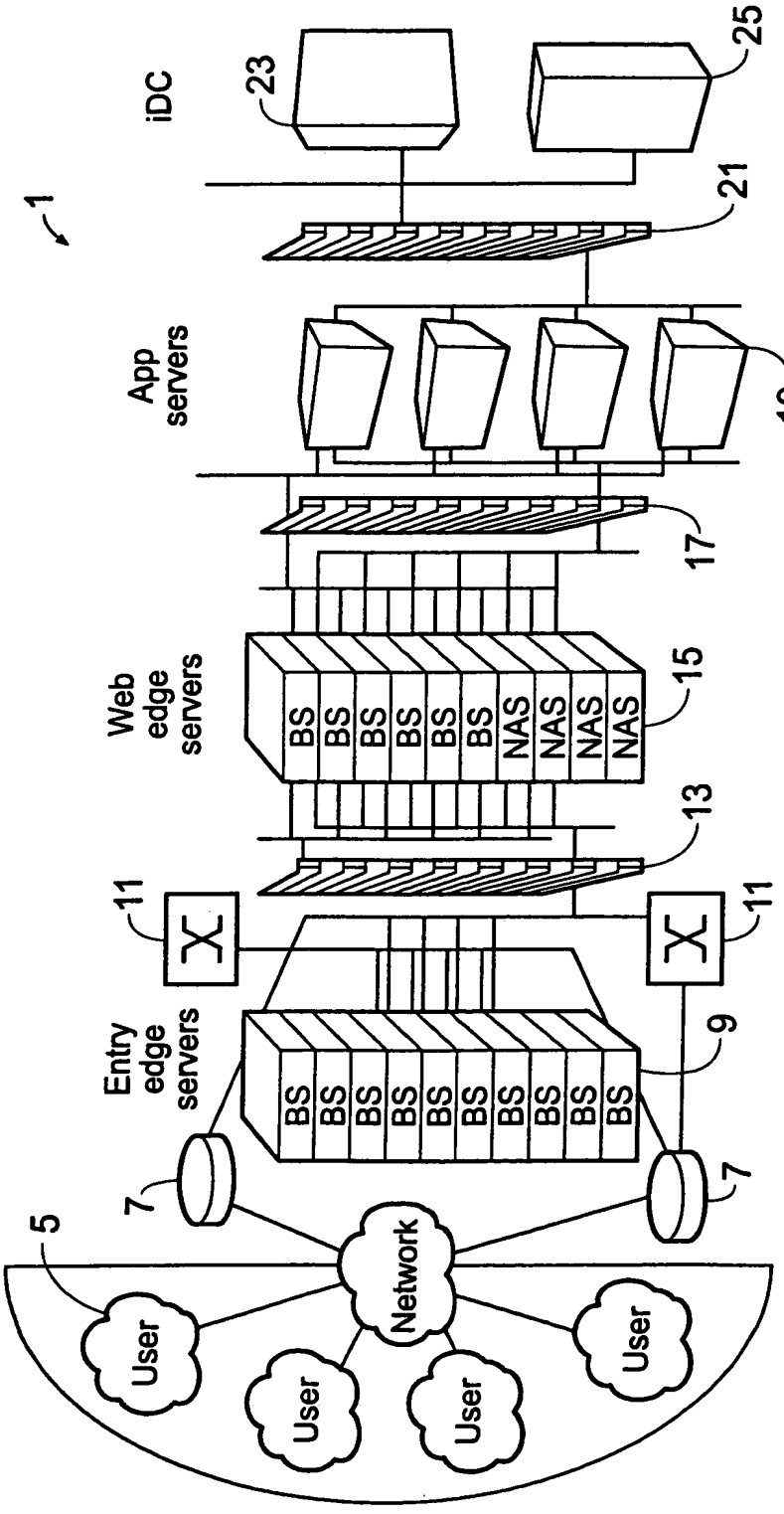


Fig. 1

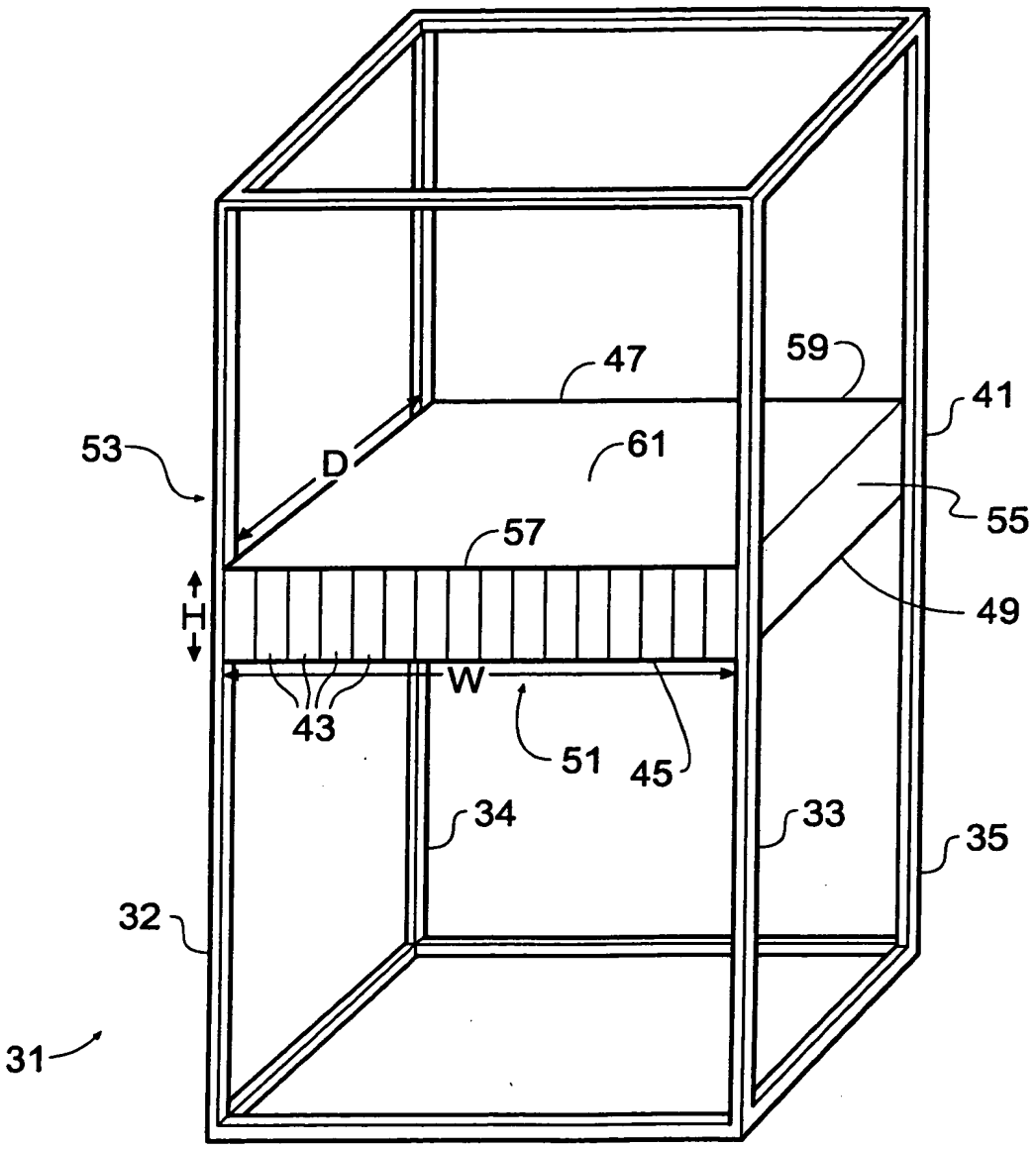


Fig. 2

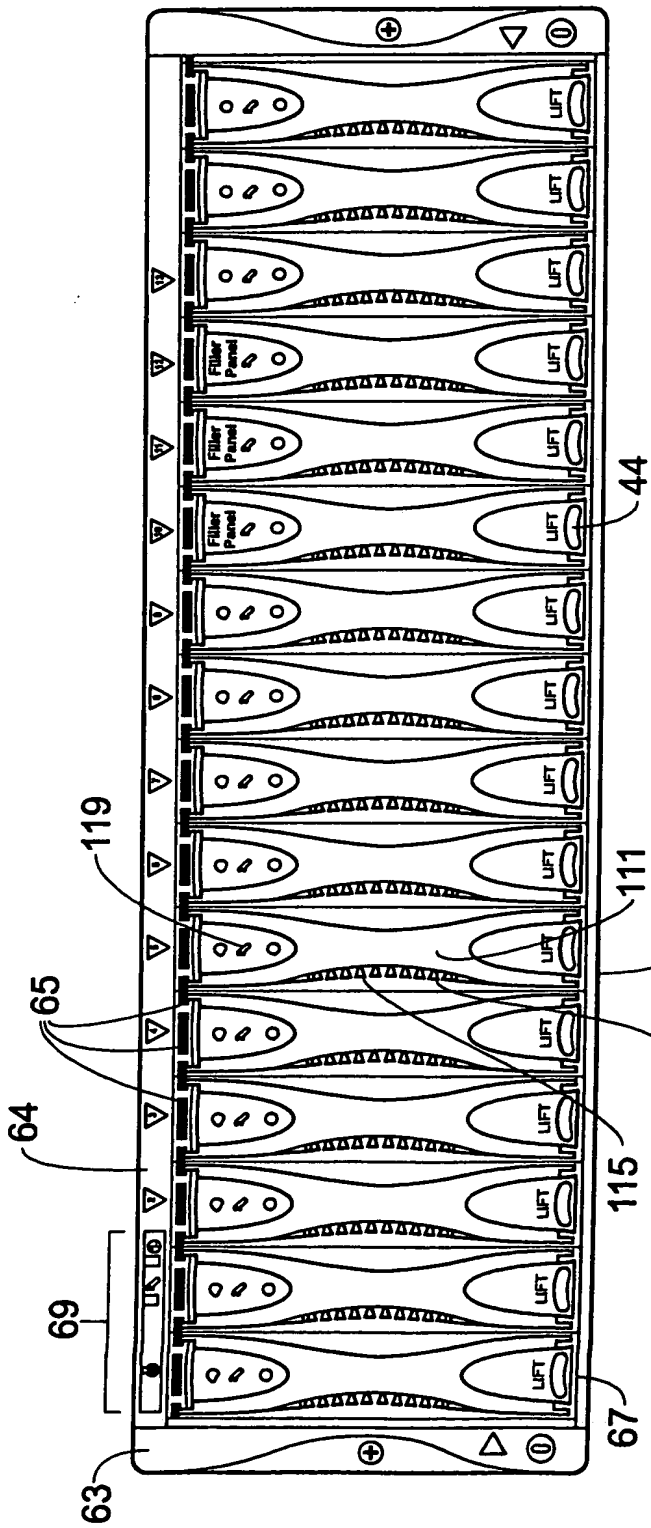


Fig. 3

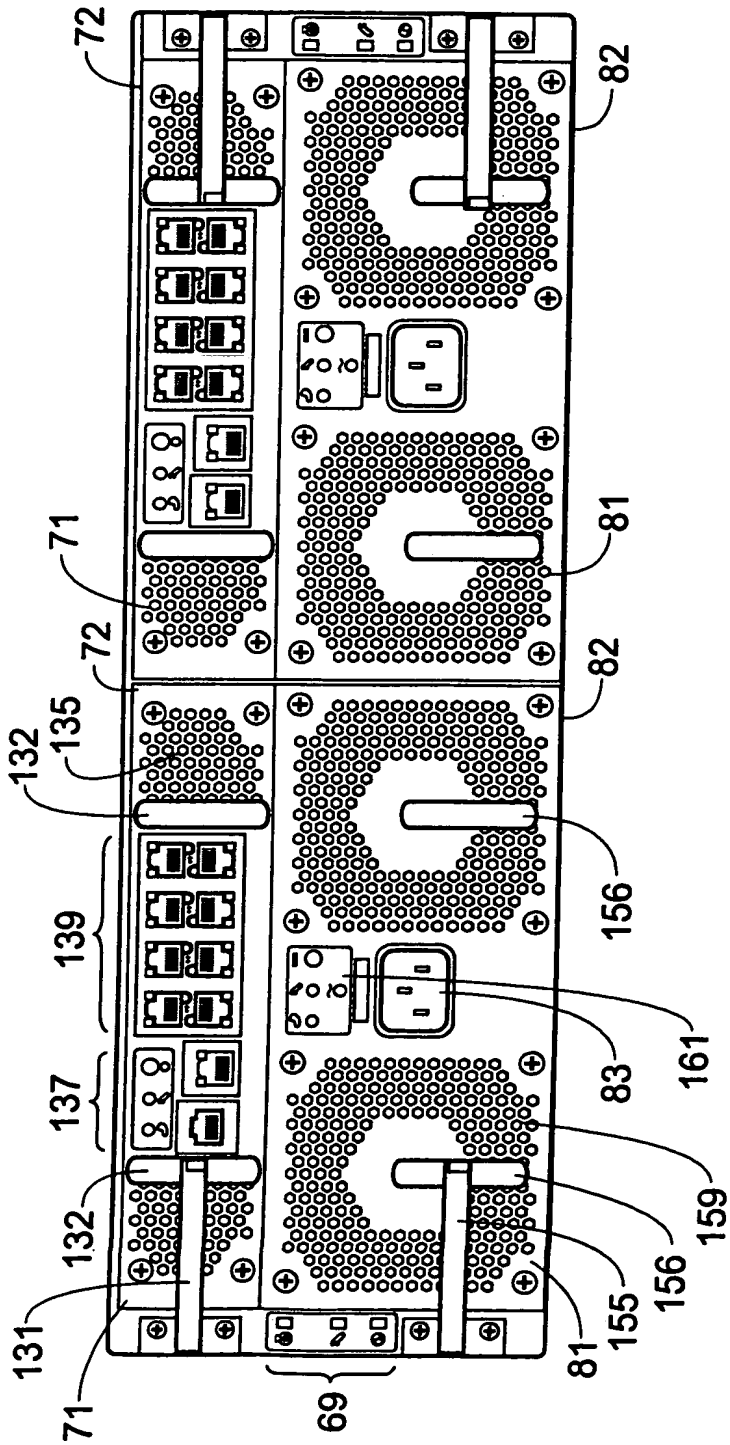

72
82
71
81
72
82
132
135
156
139
161
83
137
159
132
156
155
131
81
71
69

Fig. 4

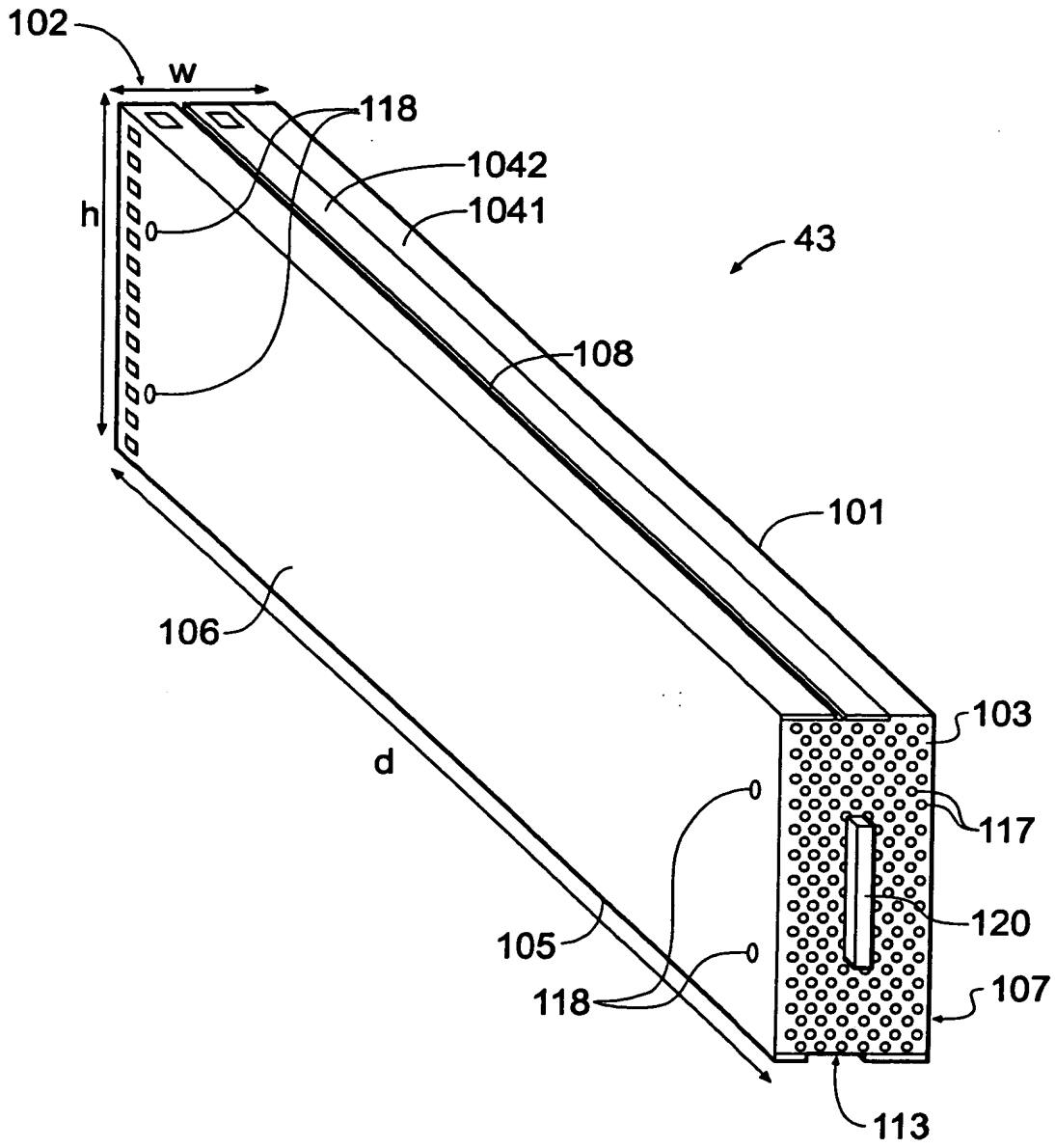


Fig. 5A

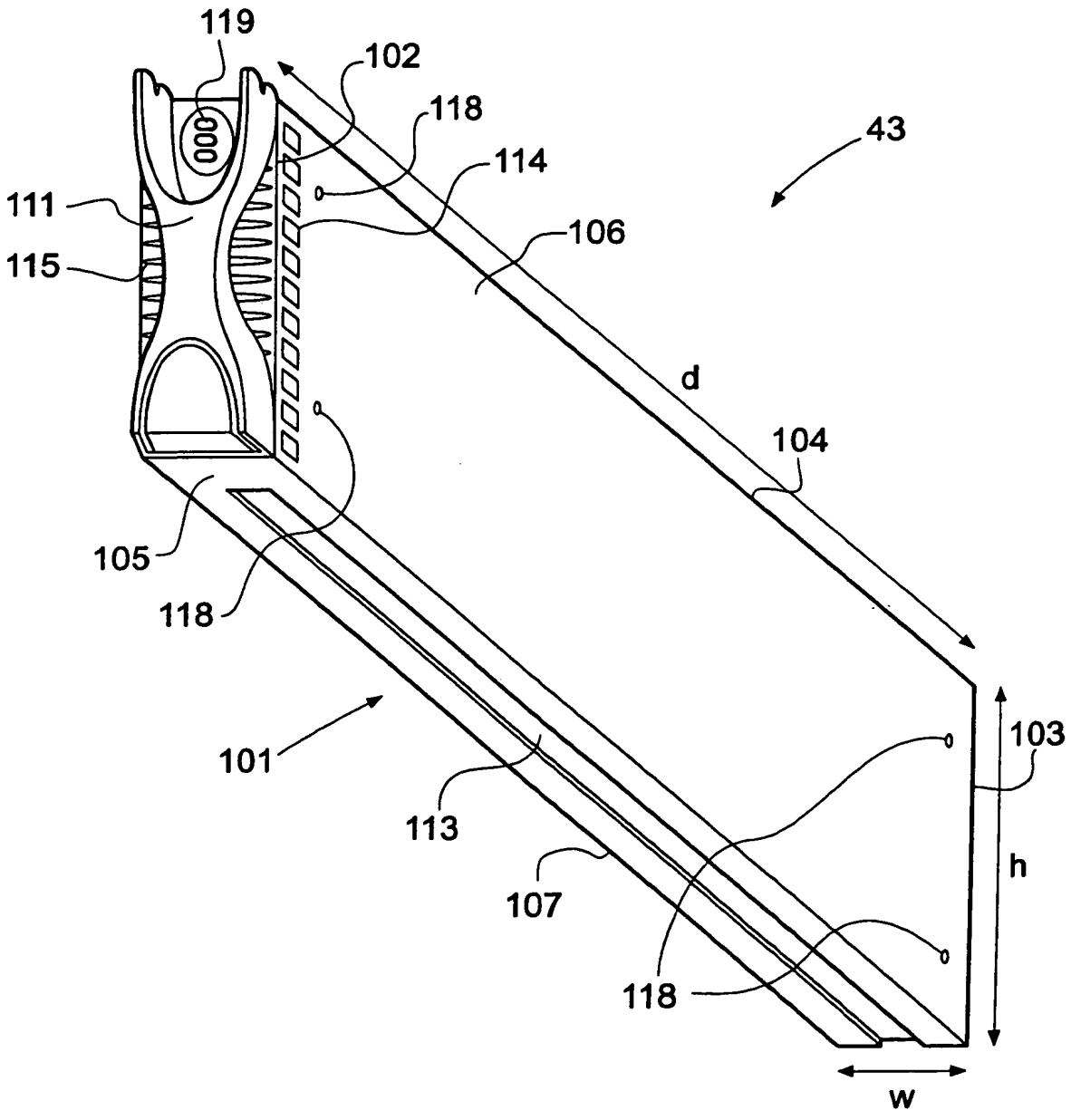

119
102
118
43
114
111
106
115
d
104
105
118
101
103
113
h
107
118
w

Fig. 5B

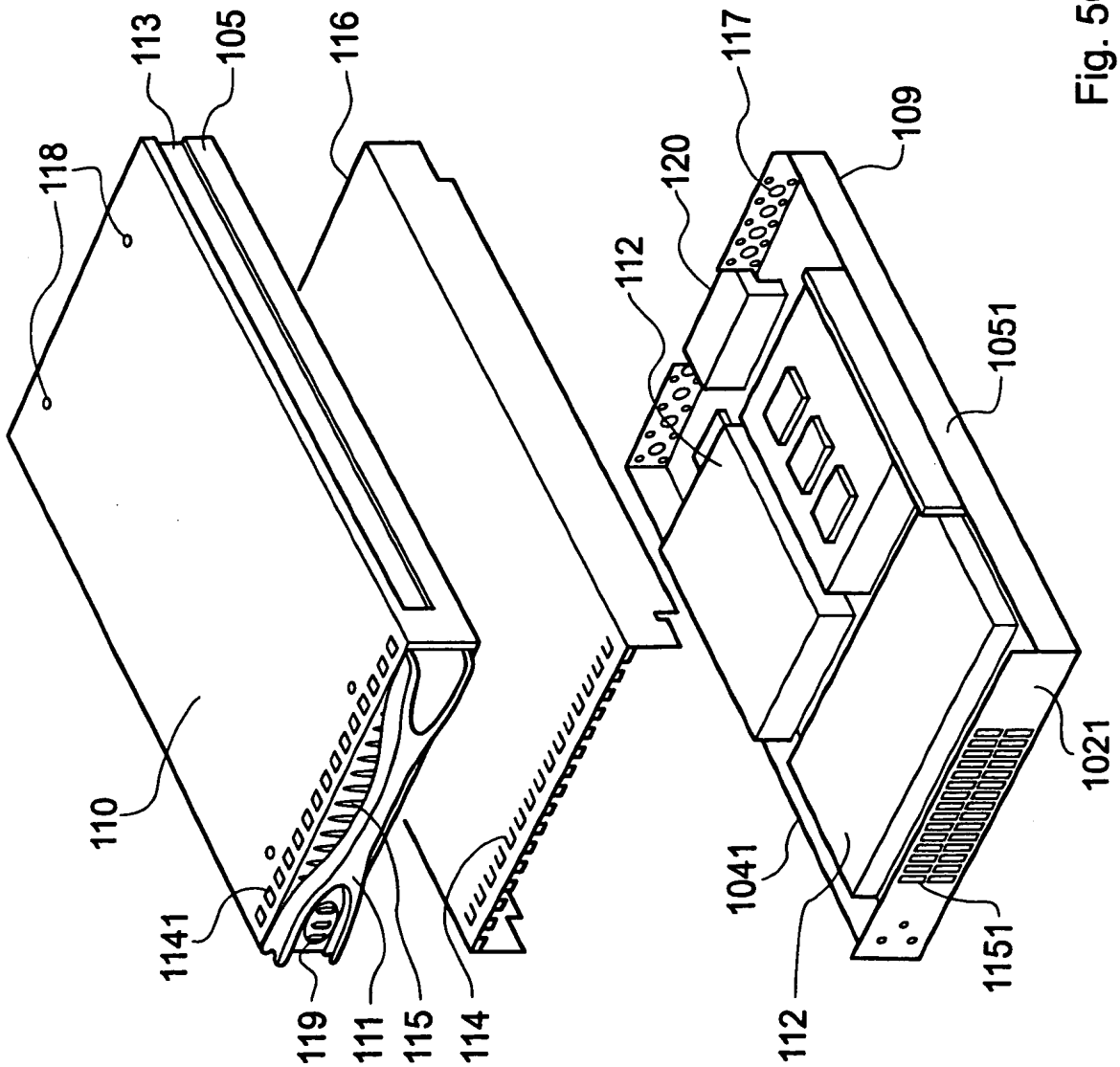

113
105
116
118
110
1141
119
111
115
114
117
109
120
112
1051
1041
112
1151
1021

Fig. 5C

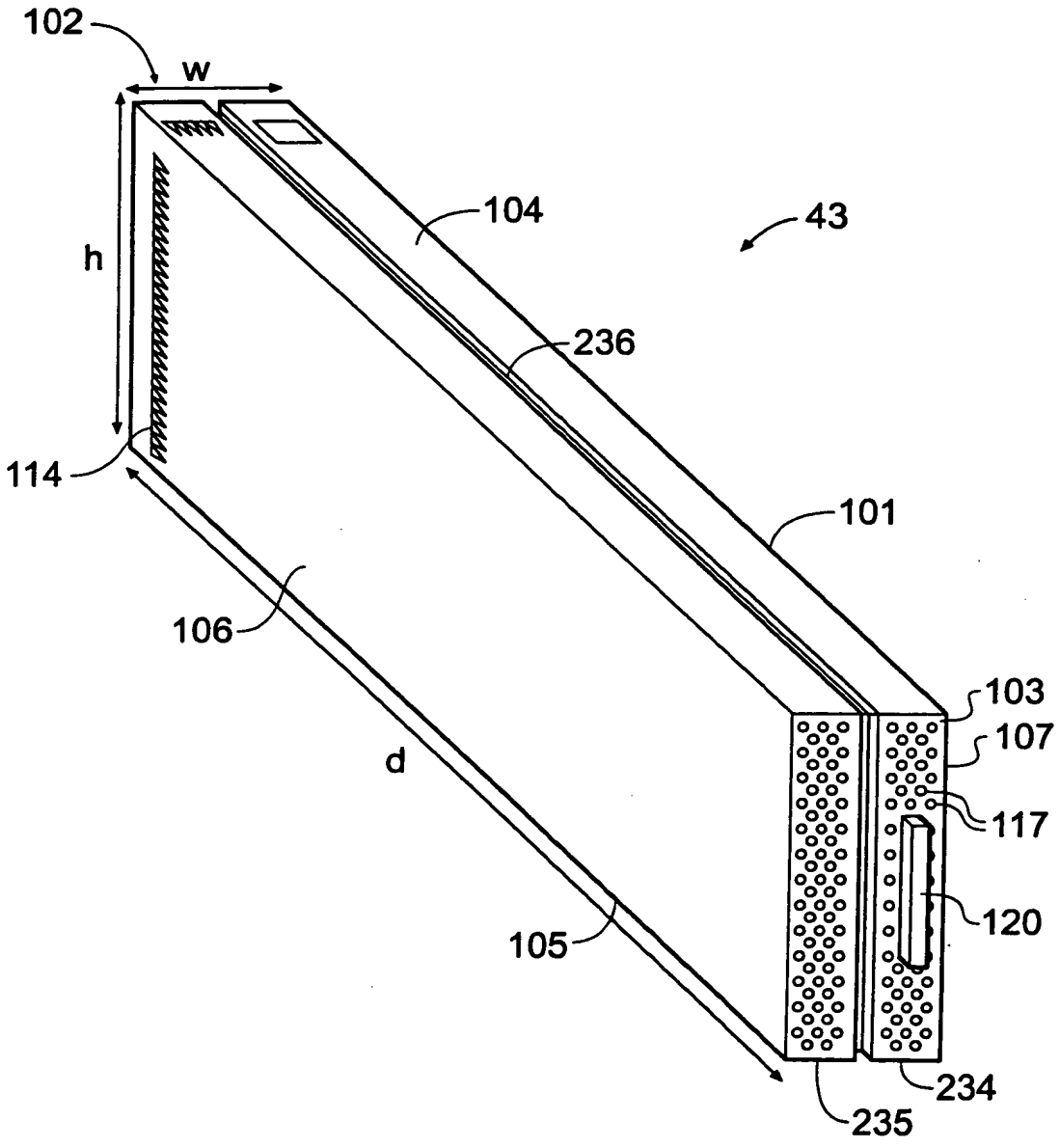


Fig. 5D

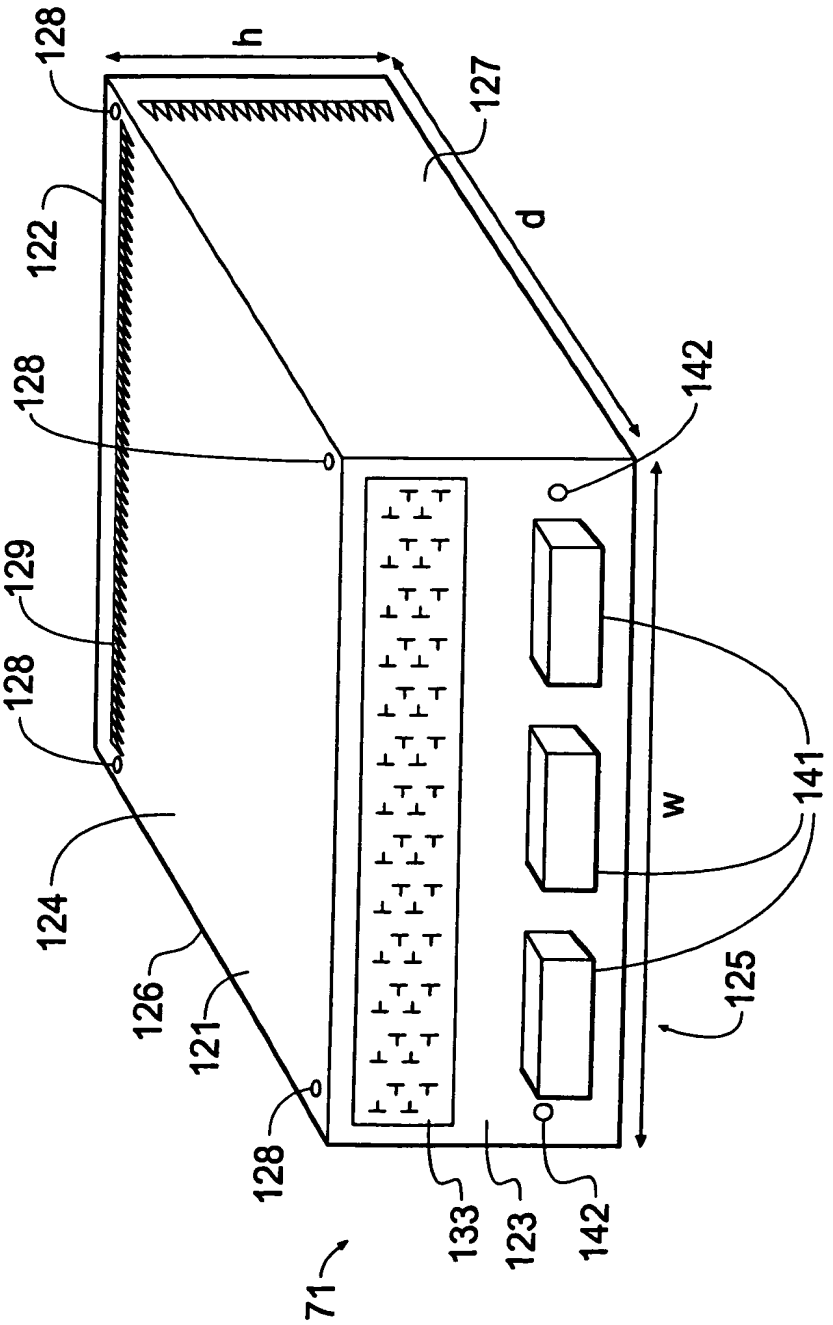

128
h
127
122
d
128
142
129
128
124
126
121
128
133
123
142
71
141
w
125

Fig. 6

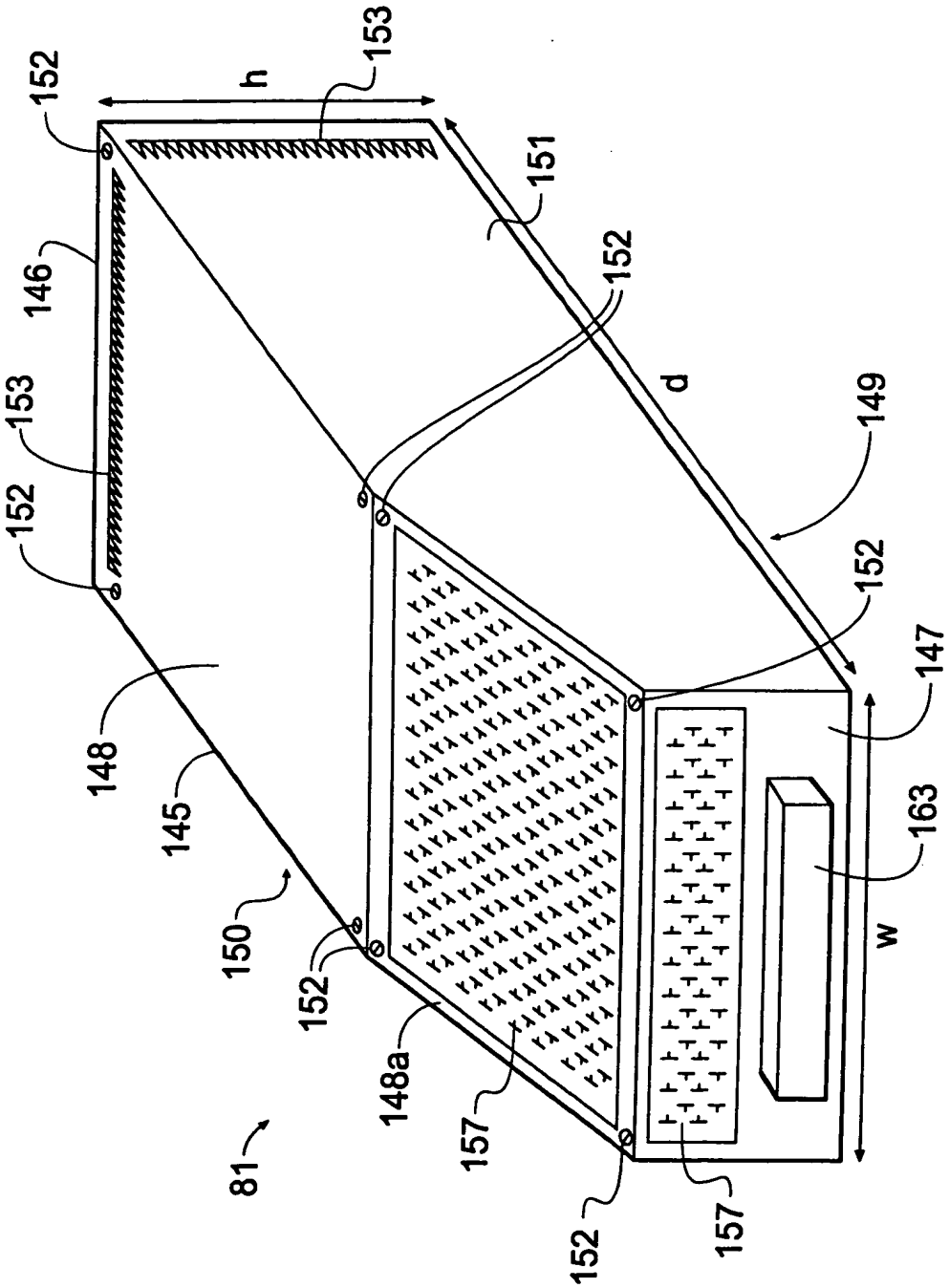

152
h
153
151
146
152
153
d
149
152
152
152
147
148
145
163
150
w
152
148a
157
81
152
157

Fig. 7

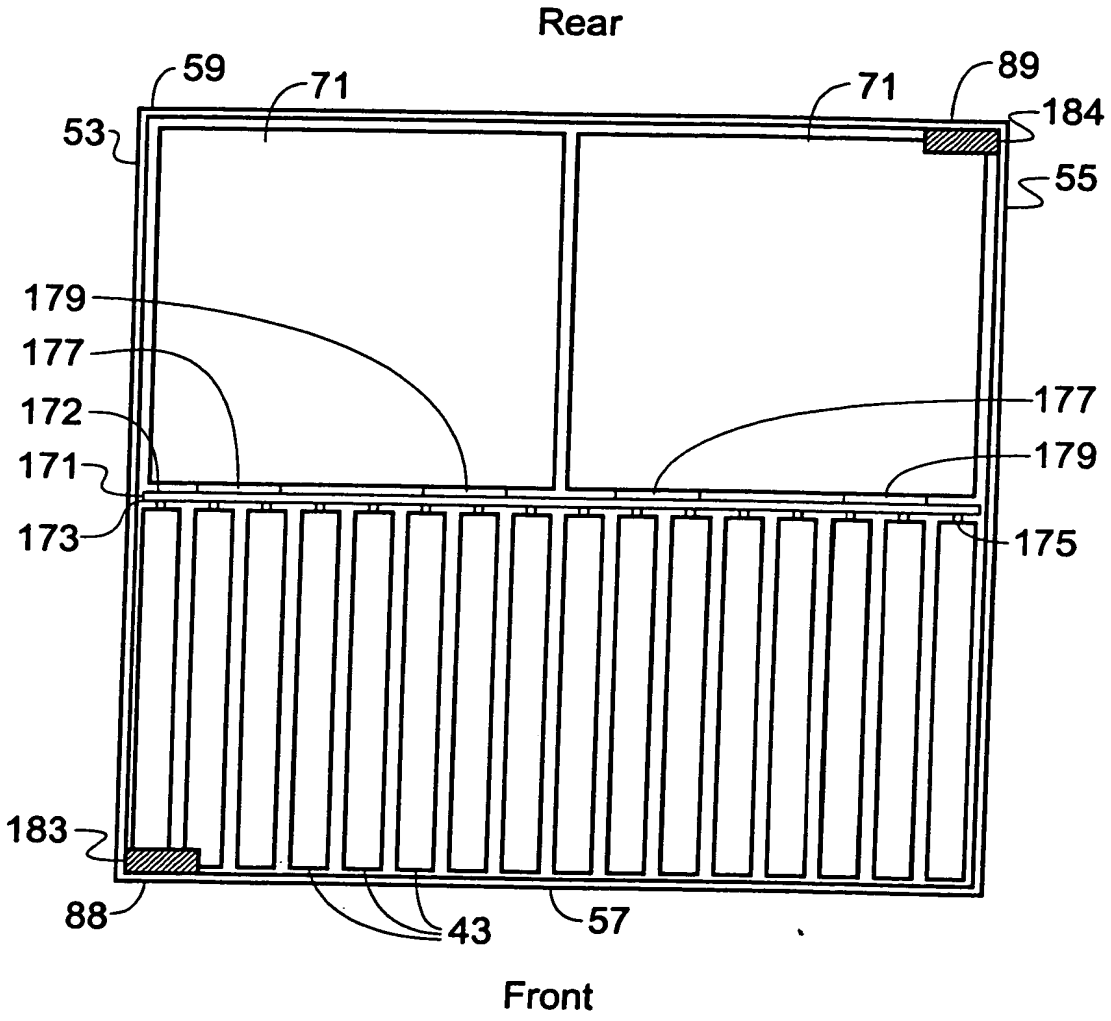

Rear
59
71
71
89
184
53
55
179
177
177
172
179
171
173
175
183
88
43
57
Front

Fig. 8A

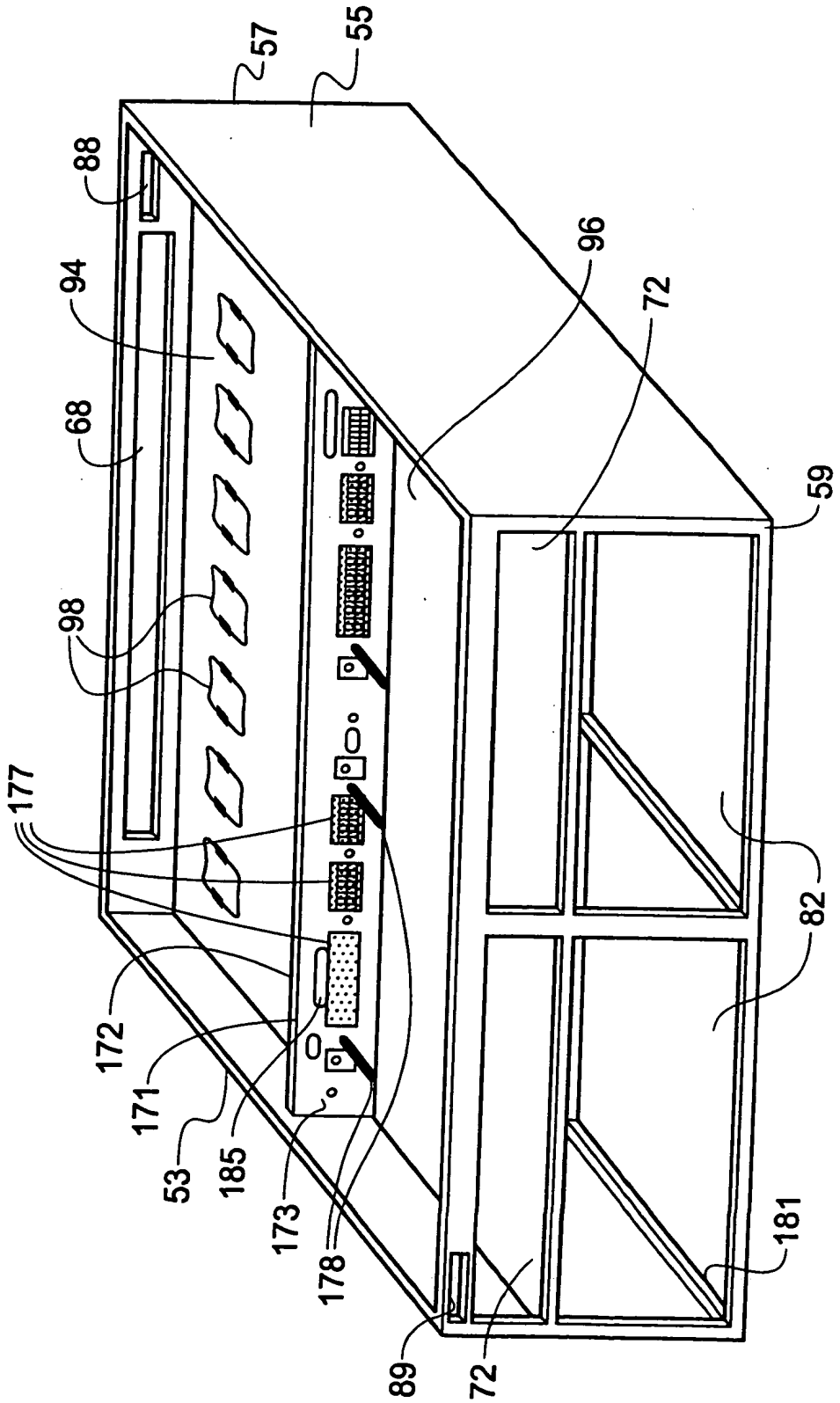


Fig. 8B

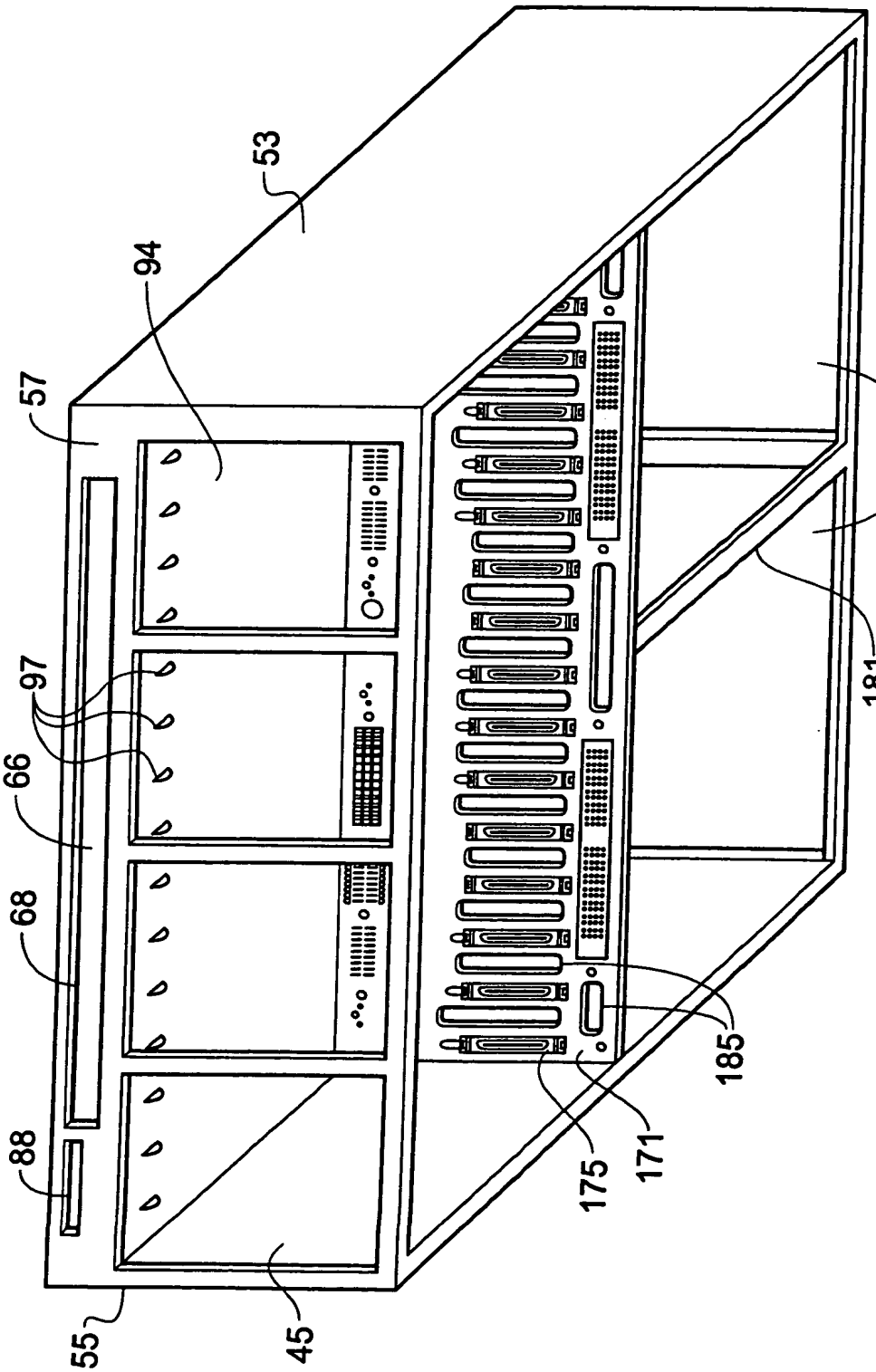


Fig. 8C

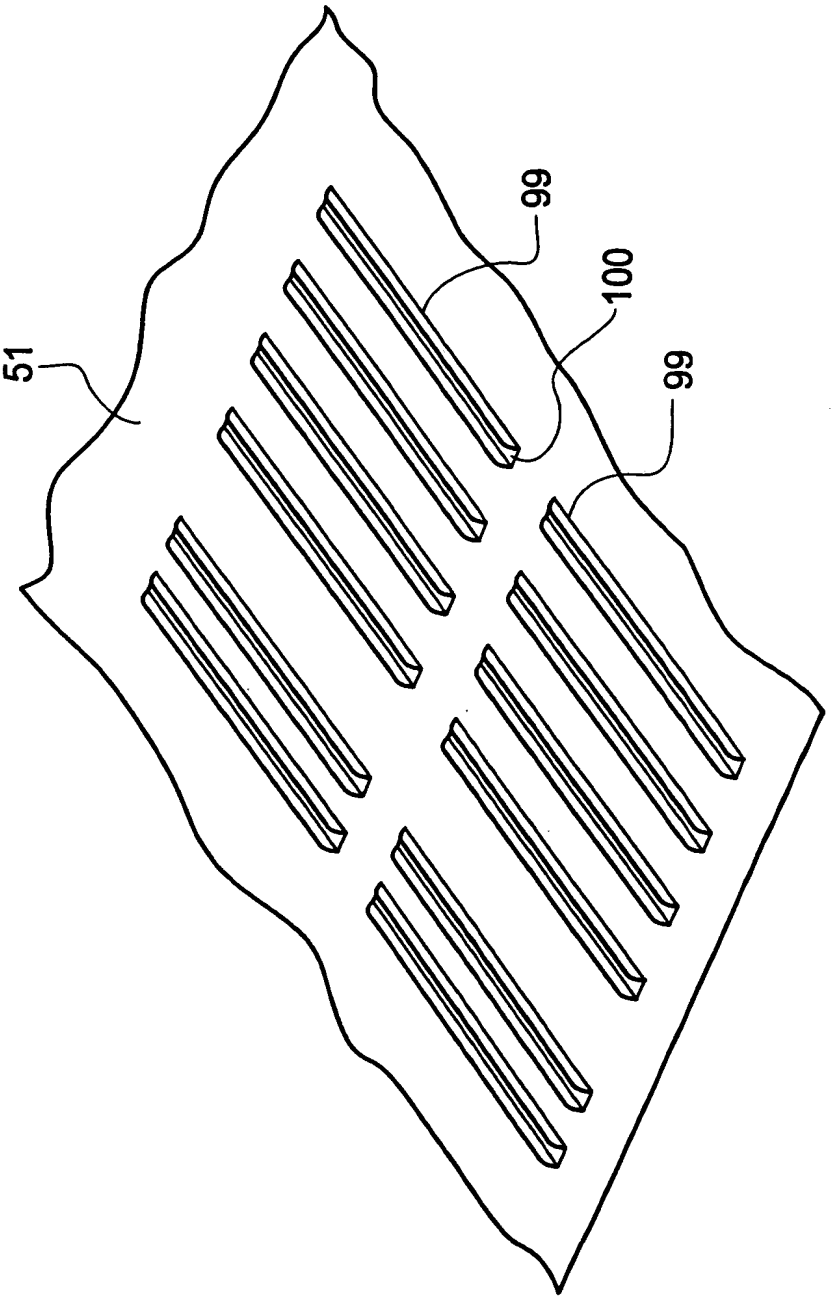


Fig. 8D

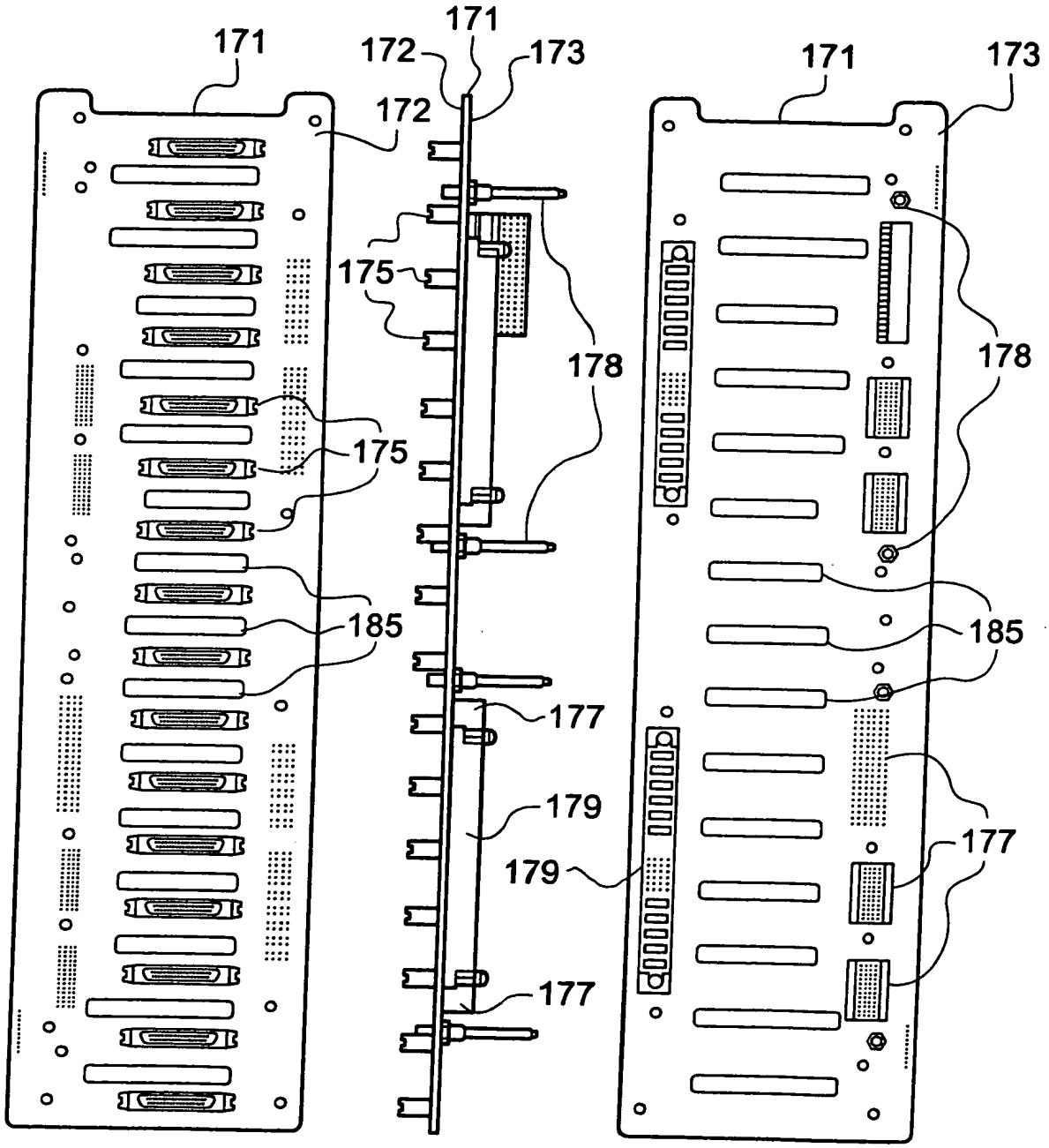


Fig. 9A Fig. 9B Fig. 9C

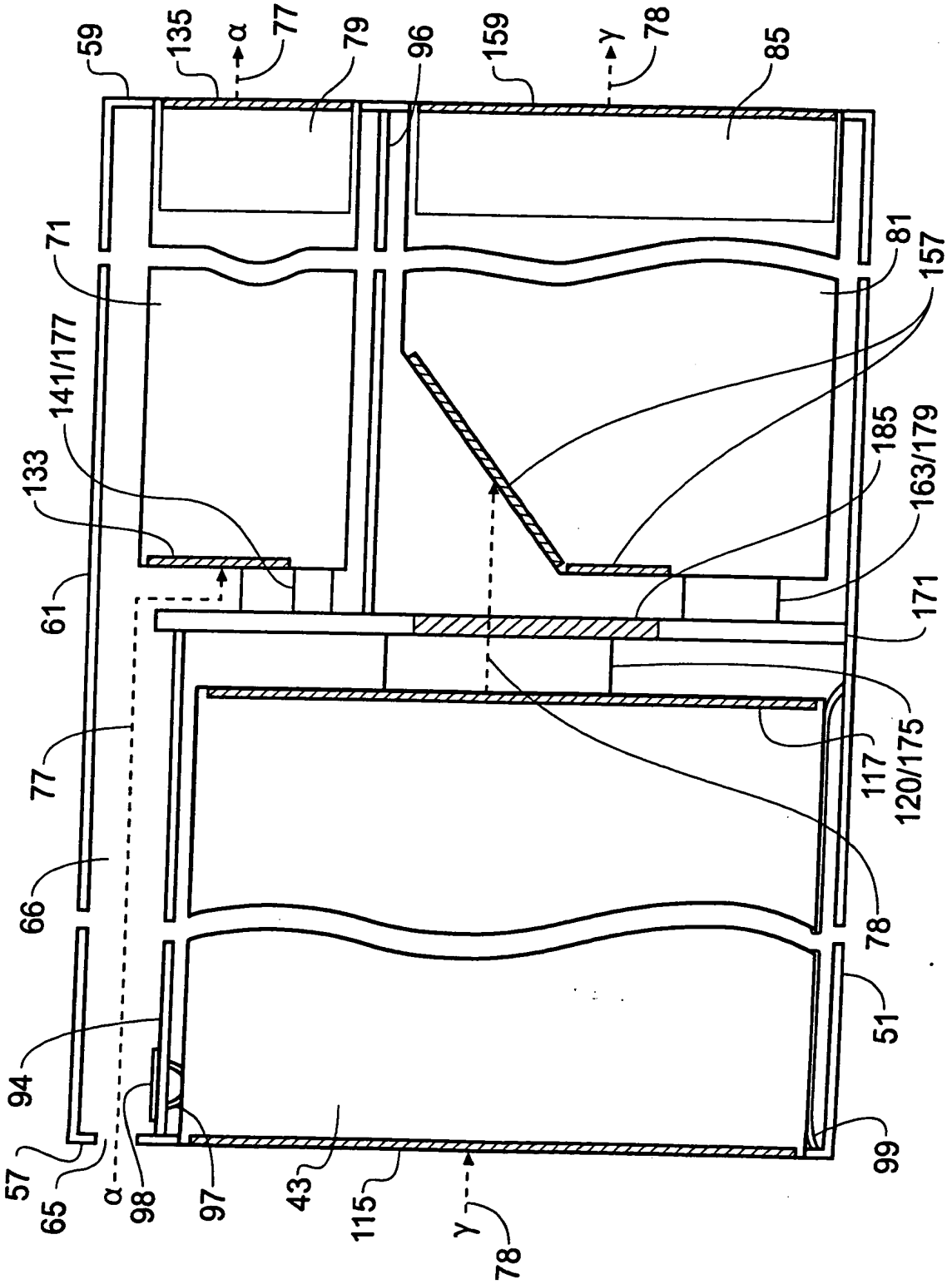

59
135
α
77
79
96
159
γ
78
85
71
81
157
141/177
133
185
163/179
61
171
77
117
120/175
66
78
94
51
57
65
α
98
97
43
115
γ
78
99

Fig. 10

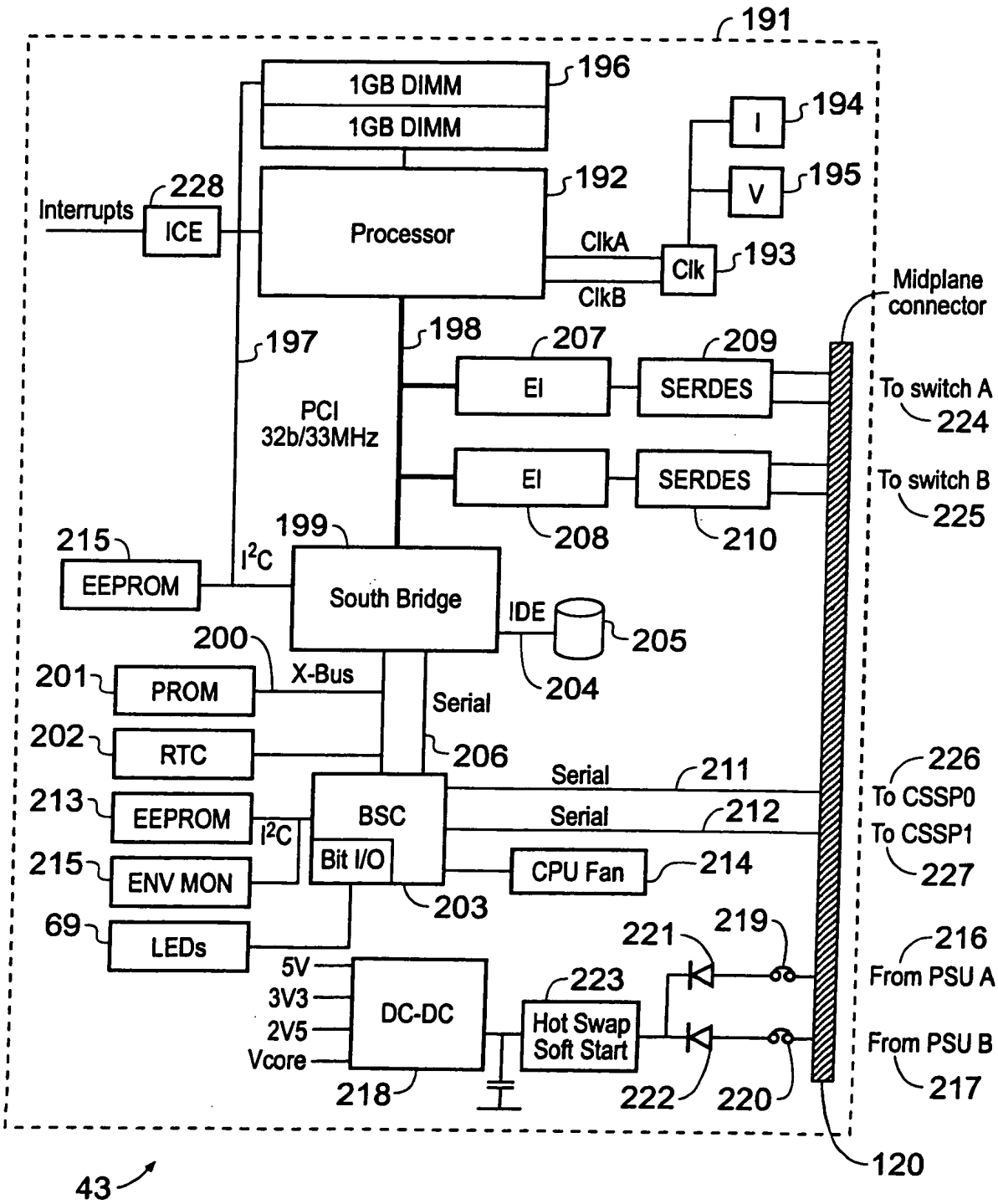
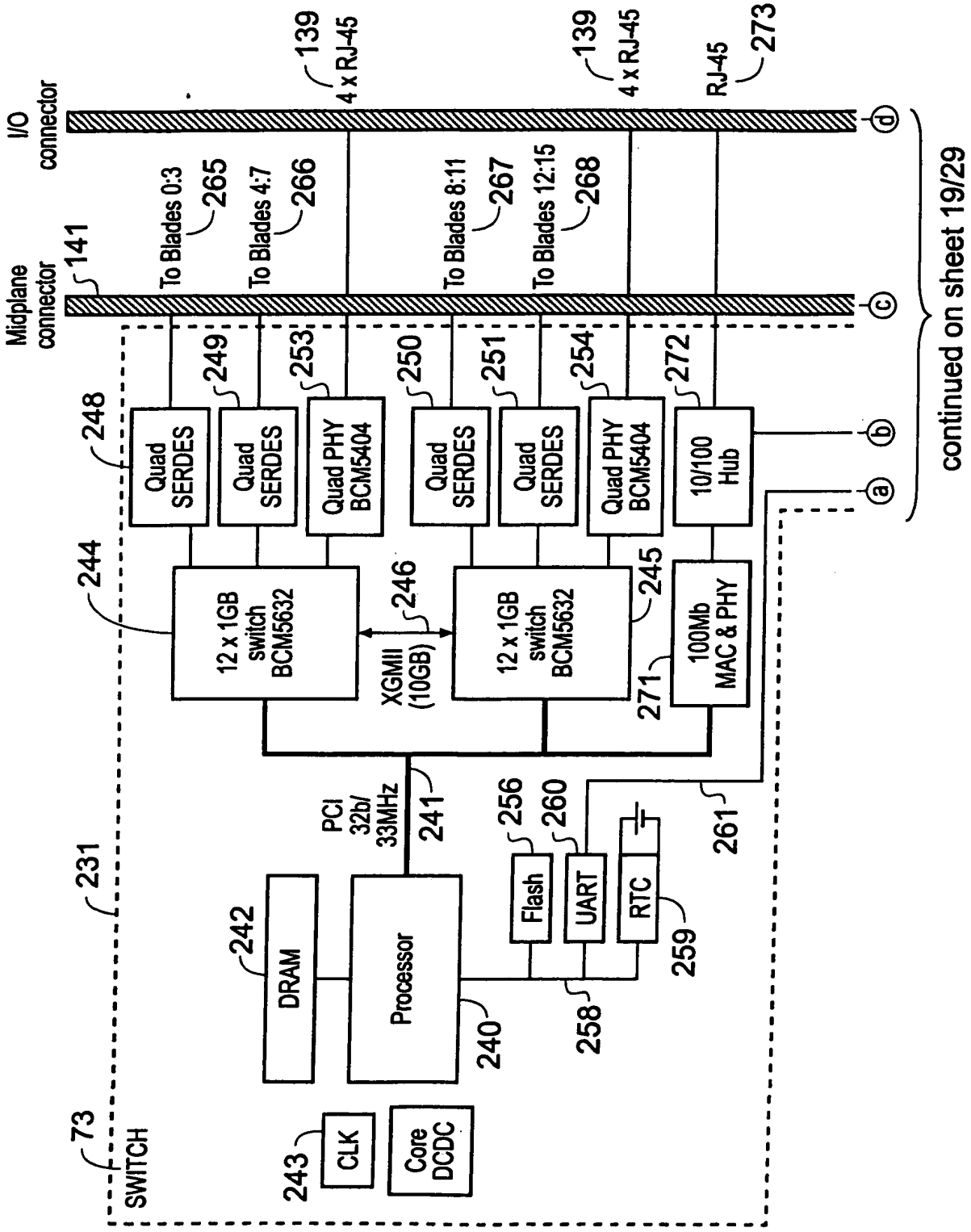

191
1GB DIMM
1GB DIMM
196
194
I
V
195
192
Processor
ClkA
ClkB
Clk
193
Interrupts
228
ICE
Midplane connector
197
198
207
209
EI
SERDES
To switch A
224
PCI 32b/33MHz
EI
SERDES
To switch B
225
208
210
215
EEPROM
I2C
199
South Bridge
IDE
205
204
200
X-Bus
201
PROM
Serial
202
RTC
206
Serial
211
226
To CSSP0
213
EEPROM
I2C
BSC
Bit I/O
Serial
212
To CSSP1
227
215
ENV MON
CPU Fan
214
203
69
LEDs
221
219
216
From PSU A
5V
3V3
2V5
Vcore
DC-DC
223
Hot Swap Soft Start
From PSU B
217
218
222
220
120
43

Fig. 11


I/O connector
139
4 x RJ-45
139
4 x RJ-45
RJ-45
273
Midplane connector
141
To Blades 0:3
265
To Blades 4:7
266
To Blades 8:11
267
To Blades 12:15
268
continued on sheet 19/29
Quad SERDES
Quad SERDES
Quad PHY BCM5404
Quad SERDES
Quad SERDES
Quad PHY BCM5404
10/100 Hub
248
249
253
250
251
254
272
244
12 x 1GB switch BCM5632
246
XGMII (10GB)
12 x 1GB switch BCM5632
245
100Mb MAC & PHY
271
PCI 32b/ 33MHz
241
261
231
242
DRAM
Processor
240
256
Flash
260
UART
RTC
259
258
243
CLK
Core DCDC
73
SWITCH

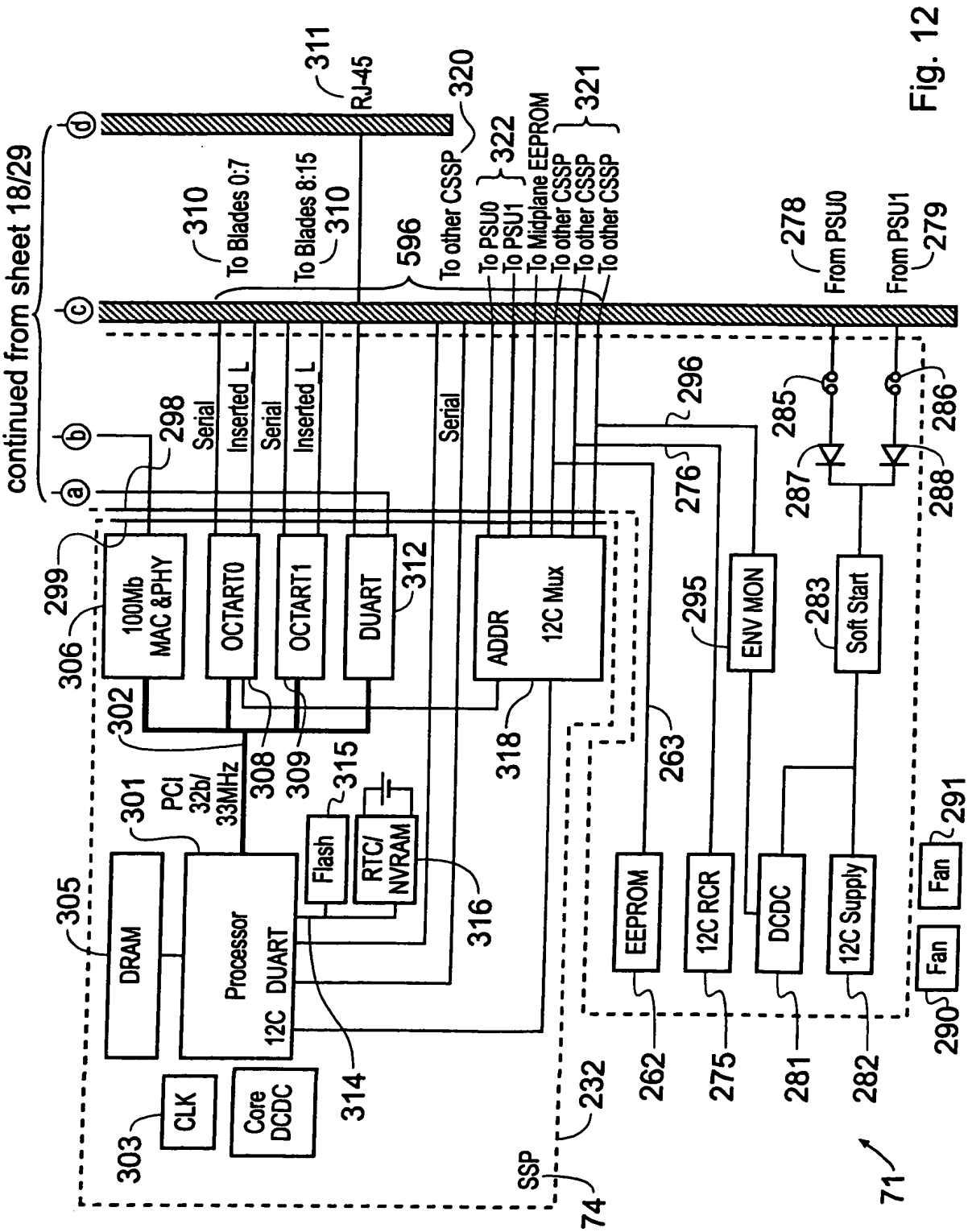

continued from sheet 18/29
a
b
c
d
298
Serial
Inserted L
Serial
Inserted L
Serial
311
RJ-45
320
To Blades 0:7
310
To Blades 8:15
310
596
To other CSSP
322
To PSU0
To PSU1
To Midplane EEPROM
321
To other CSSP
To other CSSP
To other CSSP
278
From PSU0
From PSU1
279
299
306
100Mb MAC &PHY
OCTART0
OCTART1
DUART
312
ADDR
12C Mux
296
276
285
286
287
288
295
ENV MON
283
Soft Start
302
308
309
315
318
263
301
PCI 32b/ 33MHz
Flash
RTC/ NVRAM
316
305
DRAM
Processor
12C DUART
EEPROM
12C RCR
DCDC
12C Supply
Fan
Fan
291
303
CLK
Core DCDC
314
232
262
275
281
282
290
SSP
74
71

Fig. 12

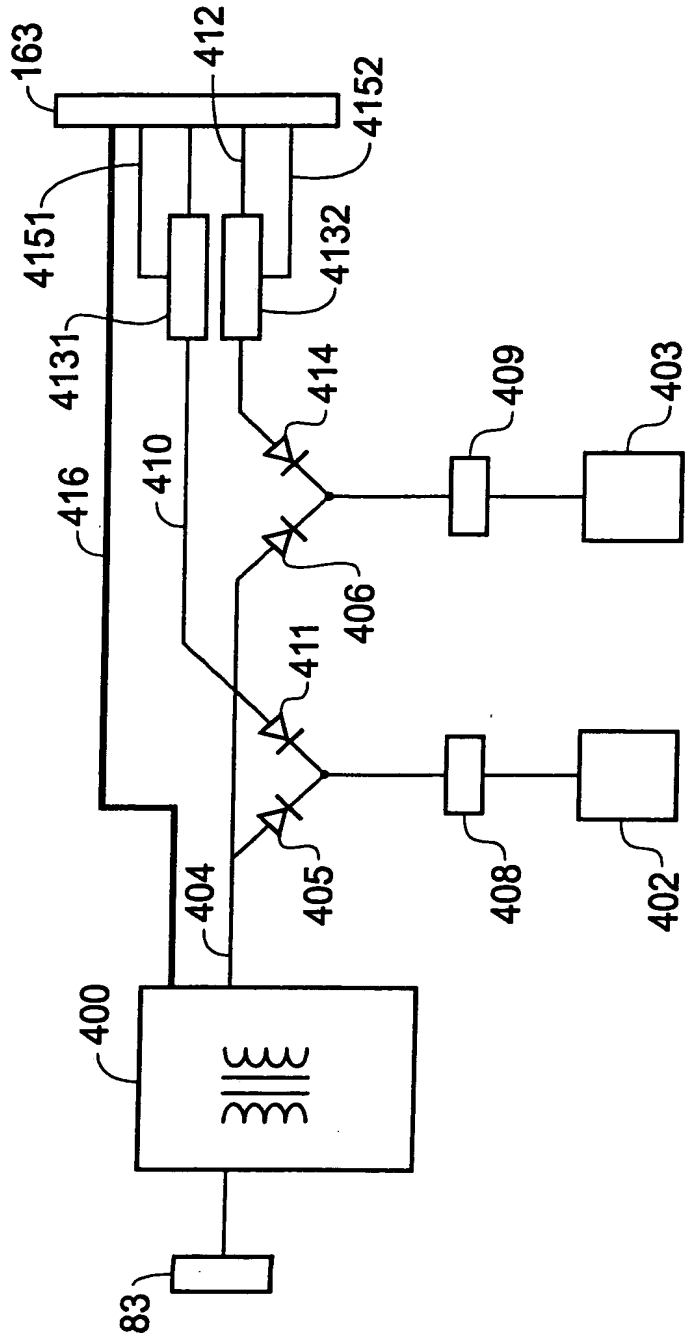

163
412
4152
4151
4132
4131
414
409
403
410
416
406
411
405
408
402
404
400
83

Fig. 13

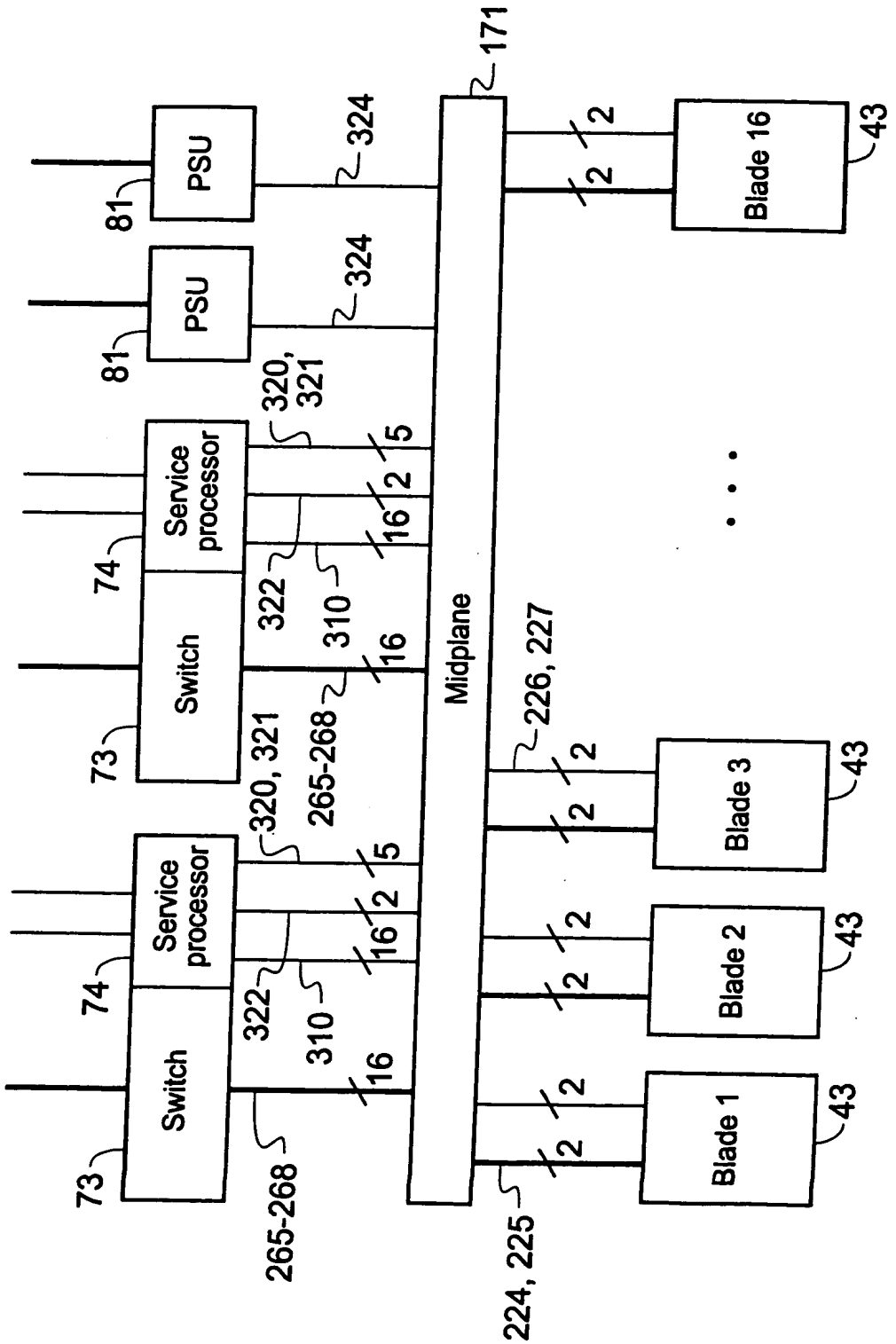

PSU
PSU
81
81
324
324
171
Midplane
Service processor
Service processor
Switch
Switch
74
74
73
73
320, 321
320, 321
322
322
310
310
265-268
265-268
16
16
5
2
2
2
2
2
2
2
2
2
2
2
226, 227
224, 225
Blade 16
Blade 3
Blade 2
Blade 1
43
43
43
43

Fig. 14

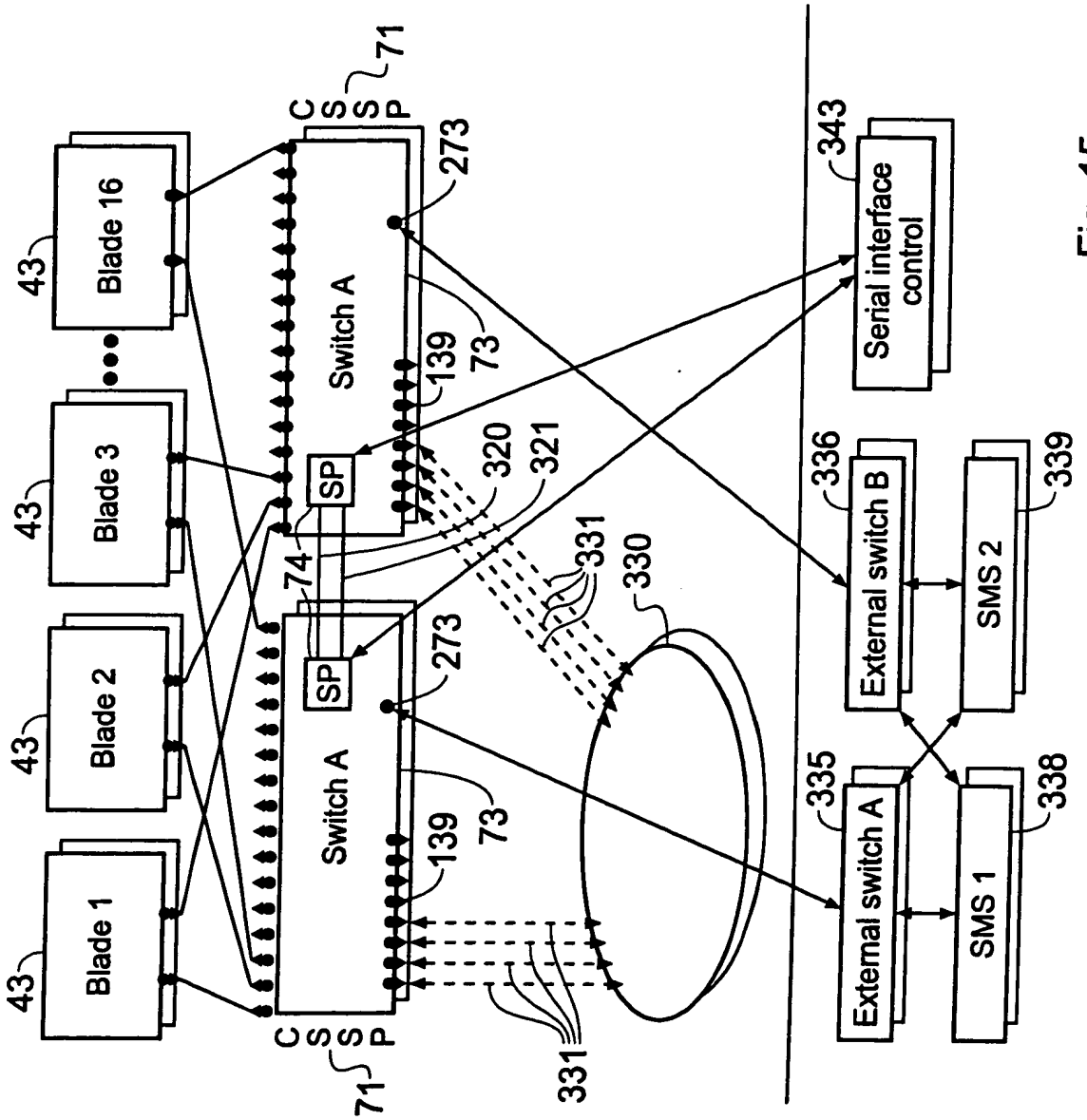

Blade 1
Blade 2
Blade 3
Blade 16
43
Switch A
SP
273
139
73
74
320
321
331
330
71
CSSP
Serial interface control
343
External switch A
External switch B
SMS 1
SMS 2
335
336
338
339

Fig. 15

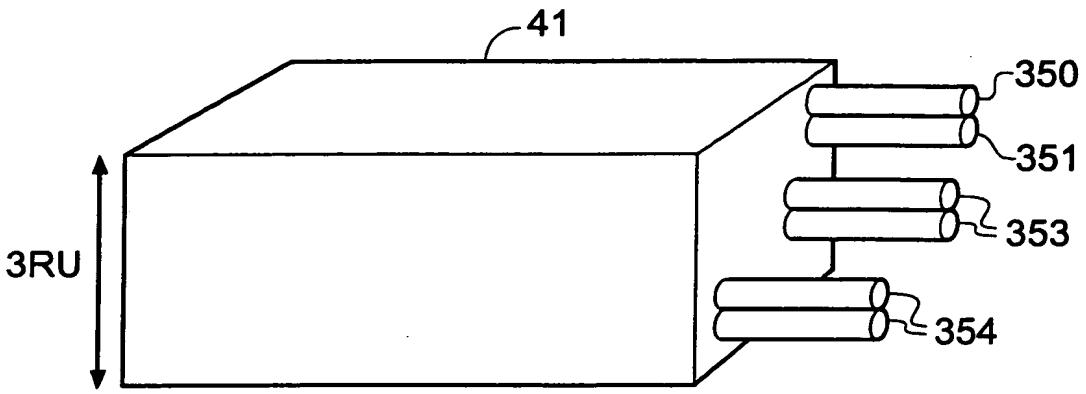


Fig. 16

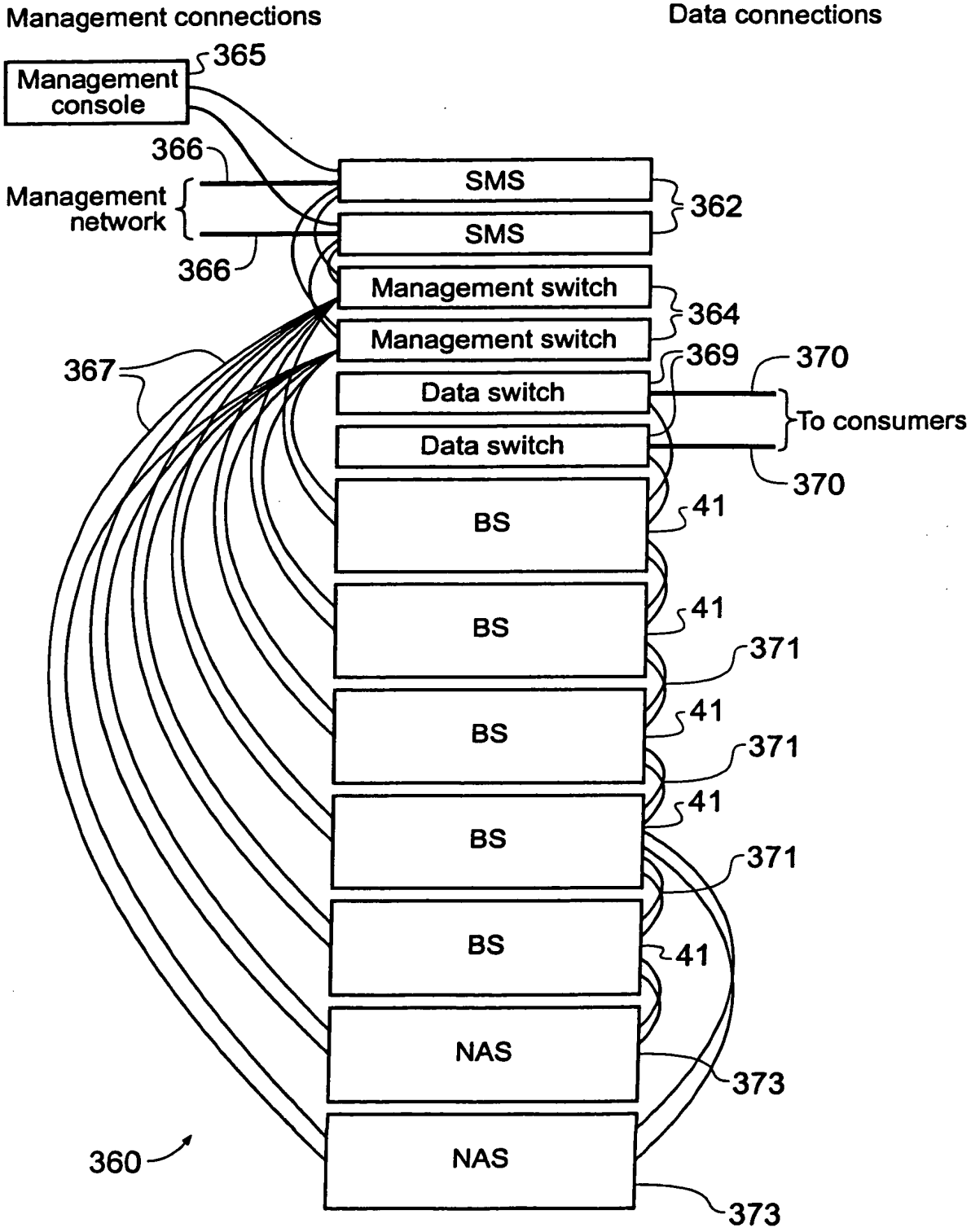

Management connections
Data connections
Management console
365
366
Management network
366
SMS
SMS
362
Management switch
Management switch
364
367
369
370
Data switch
Data switch
To consumers
370
BS
41
BS
41
371
BS
41
371
BS
41
371
BS
41
NAS
373
NAS
373
360

Fig. 17

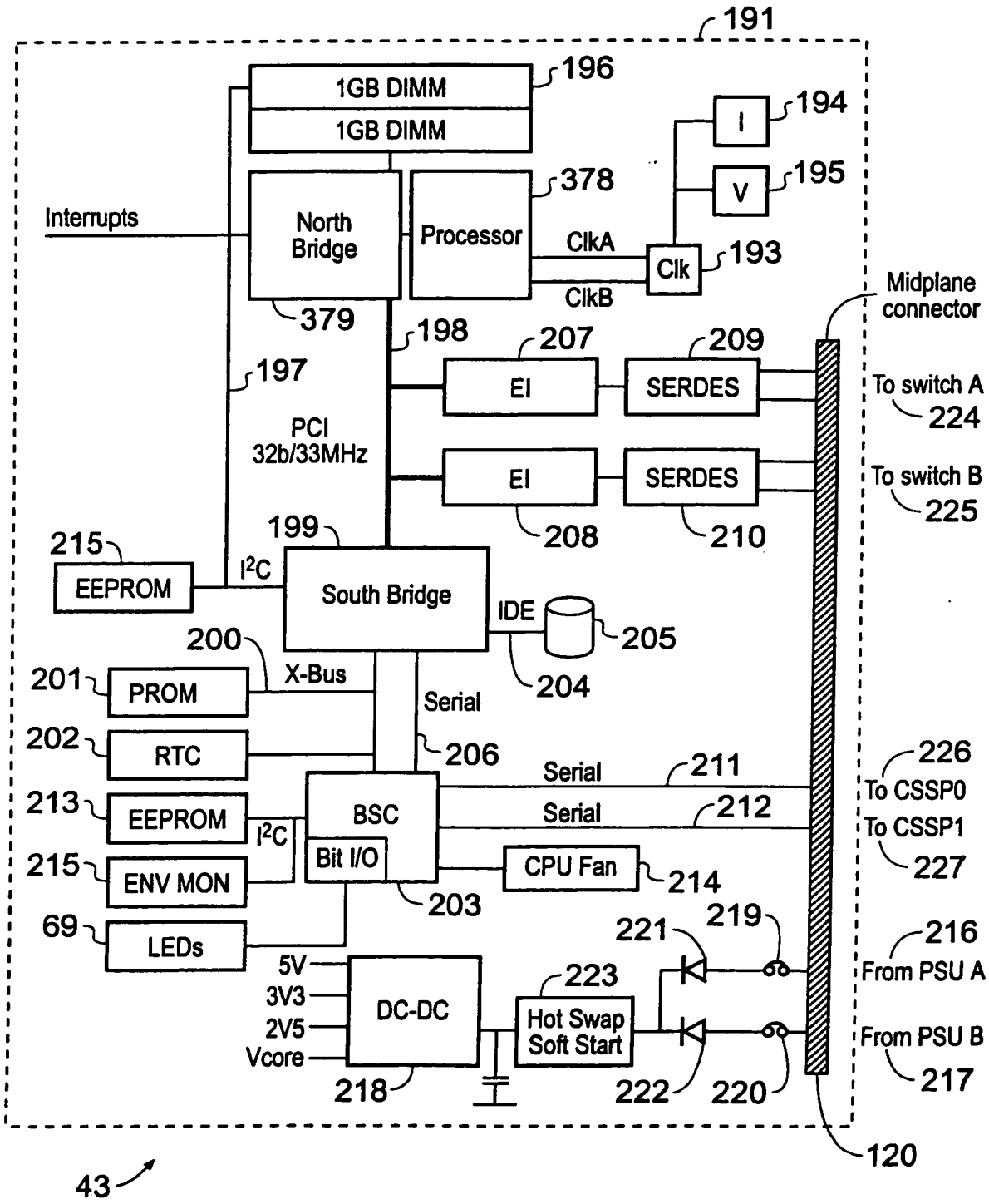

191
1GB DIMM
1GB DIMM
196
I
194
V
195
378
Interrupts
North Bridge
Processor
ClkA
ClkB
Clk
193
379
Midplane connector
198
207
209
197
EI
SERDES
To switch A
224
PCI 32b/33MHz
EI
SERDES
To switch B
225
208
210
199
215
EEPROM
I2C
South Bridge
IDE
205
200
204
201
PROM
X-Bus
Serial
202
RTC
206
226
Serial
211
To CSSP0
213
EEPROM
I2C
BSC
Serial
212
To CSSP1
Bit I/O
215
ENV MON
CPU Fan
214
227
203
69
LEDs
221
219
216
5V
3V3
2V5
Vcore
DC-DC
223
Hot Swap Soft Start
From PSU A
From PSU B
217
218
222
220
120
43

Fig. 18

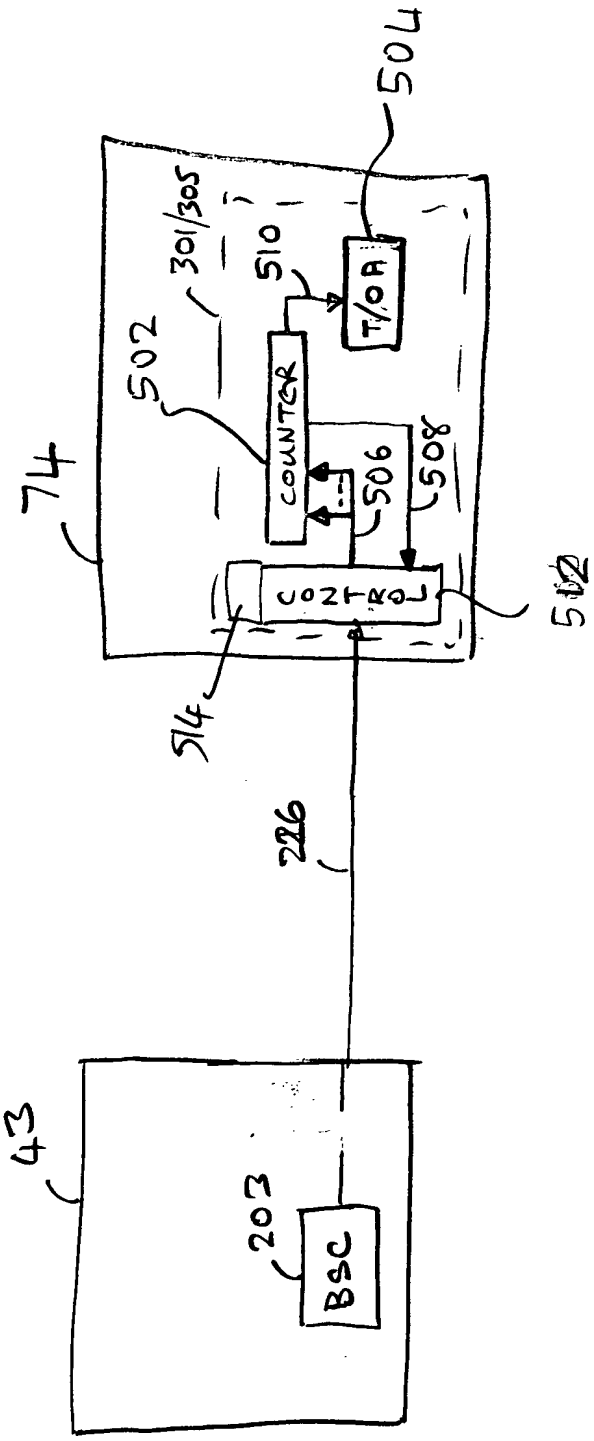

504
301/305
510
T/OA
502
COUNTER
506
508
74
CONTROL
512
514
226
43
203
BSC

FIG 19

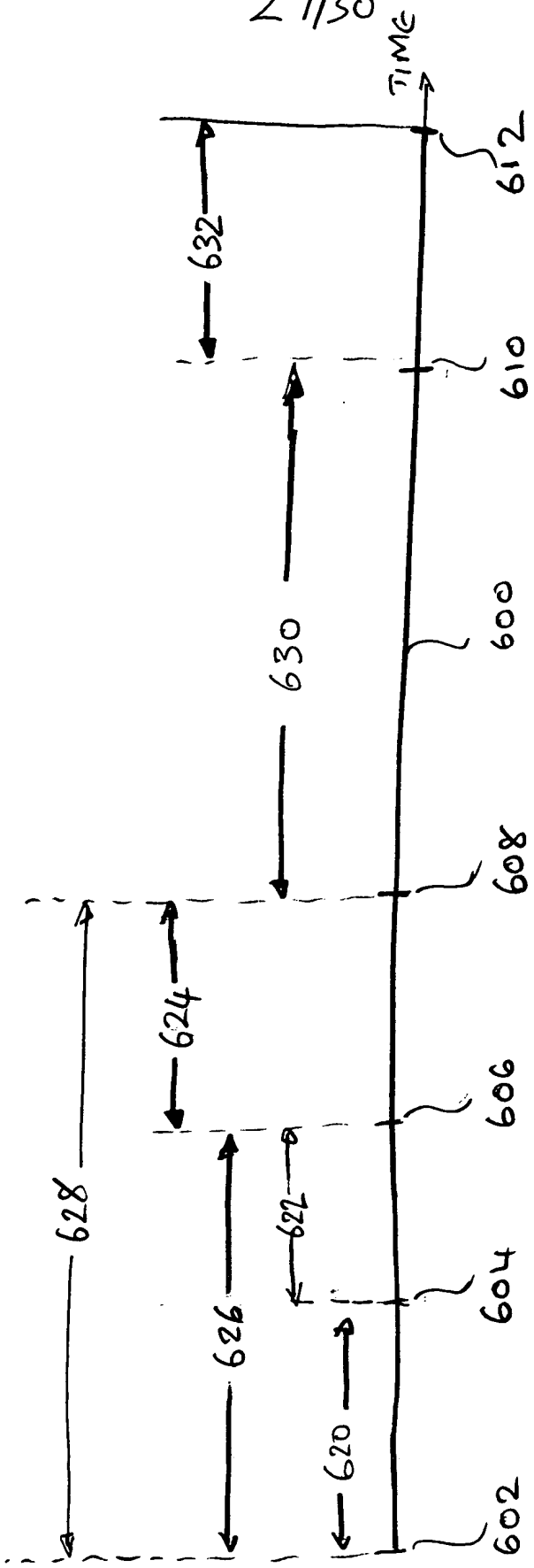


FIG 20

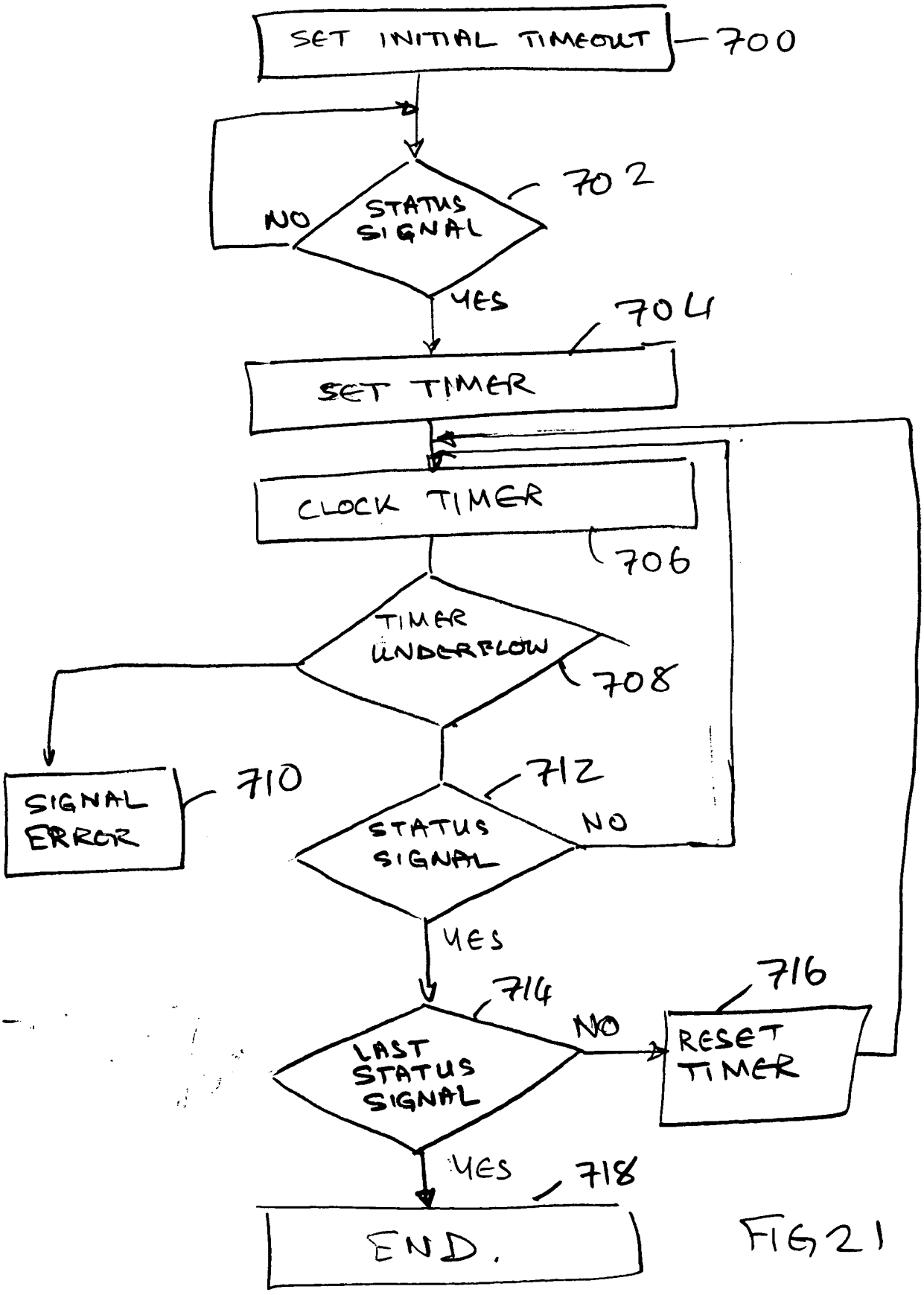

SET INITIAL TIMEOUT
700
STATUS SIGNAL
702
NO
YES
SET TIMER
704
CLOCK TIMER
706
TIMER UNDERFLOW
708
SIGNAL ERROR
710
STATUS SIGNAL
712
NO
YES
LAST STATUS SIGNAL
714
NO
RESET TIMER
716
YES
718
END.

FIG 21

BLADE BOOT Ø (1 YEAR)

↓ USER SETTING 5 HOURS

BLADE BOOT 1 = 1.5 MIN

↓ TIMEOUT 1 HOUR

BLADE BOOT 2 = 1.2 Min

↓ TIMEOUT = 10 MINS.

BLADE BOOT 3

↓ ETC.

FIG 22

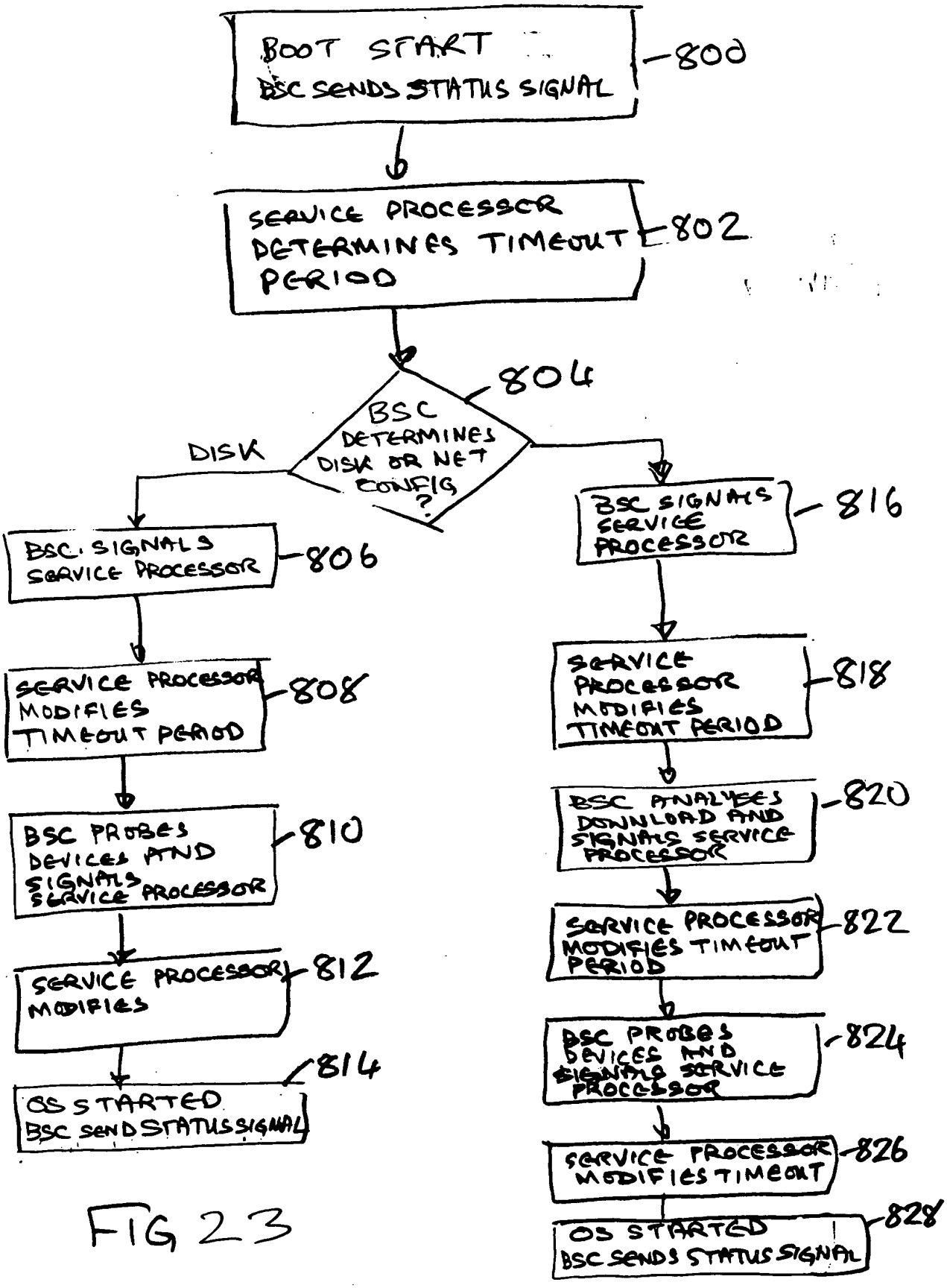

BOOT START
BSC SENDS STATUS SIGNAL
800
SERVICE PROCESSOR DETERMINES TIMEOUT PERIOD
802
804
BSC DETERMINES DISK OR NET CONFIG ?
DISK
BSC SIGNALS SERVICE PROCESSOR
806
SERVICE PROCESSOR MODIFIES TIMEOUT PERIOD
808
BSC PROBES DEVICES AND SIGNALS SERVICE PROCESSOR
810
SERVICE PROCESSOR MODIFIES
812
OS STARTED BSC SEND STATUS SIGNAL
814
BSC SIGNALS SERVICE PROCESSOR
816
SERVICE PROCESSOR MODIFIES TIMEOUT PERIOD
818
BSC ANALYSES DOWNLOAD AND SIGNALS SERVICE PROCESSOR
820
SERVICE PROCESSOR MODIFIES TIMEOUT PERIOD
822
BSC PROBES DEVICES AND SIGNALS SERVICE PROCESSOR
824
SERVICE PROCESSOR MODIFIES TIMEOUT
826
OS STARTED BSC SENDS STATUS SIGNAL
828

FIG 23